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# 18. A LOW-NOISE PHASE-LOCKED-OSCILLATOR MULTIPLIER

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A 100-Mc crystal oscillator can be phase-locked to any submultiple frequency between 1 and 10 Mc/sec. The use of a keyed phase detector makes it possible to obtain a wide range of multiplication ratios without adjustments of the circuit. Exceptional flexibility for experimental purposes and large multiplication ratios in a single stage are obtained with only moderate complexity. The bandwidth of the multiplier can be made over 5 kc/sec wide at 100 Mc/sec, so that the characteristics of the driving source are reproduced for averaging times down to less than 100 μsec. The noise level of the multiplier is less than −145 db per cps bandwidth at the 100-Mc output.

Figure 18–1 is a block diagram of the multiplier. A short pulse, generated at the input frequency, keys the phase detector. The output from the phase detector is proportional to the amplitude of the 100-Mc signal when the input pulse is generated. This output is used to correct the frequency of the crystal oscillator. This arrangement permits any integral ratio between output and input frequency (e.g., if the ratio is 20, every 20th cycle is sampled; if the ratio is 100, every 100th cycle is sampled). As long as the pulse

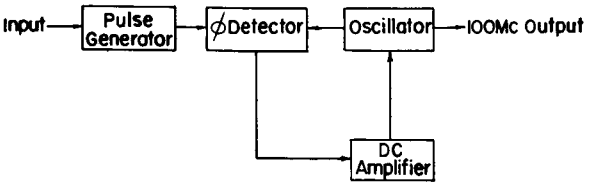


FIGURE 18–1.—Phase-locked oscillator multiplier (PLOM).

generator (Figure 18–2) can produce pulses at the input frequency and the loading on the detector is negligible, there is no theoretical limit on frequency ratio. Very high ratios have been successfully used in experimental units (Reference 1).

Figure 18–3 is a simplified diagram of the phase detector. Several factors limit the frequency ratio: (1) The pulse must be shorter than $\frac{1}{2}$ cycle of the waveform to be sampled, (2) the source impedance of the high-frequency signal and the "on" resistance of the switch $S$ must be low enough to charge the holding capacitor $C_H$ during one sample, and (3) the load impedance across $C_H$ must be high enough to prevent decay of voltage across $C_H$ between samples. The larger $C_H$ is, the longer is the holding (discharge) time constant; but the source impedance must be lower

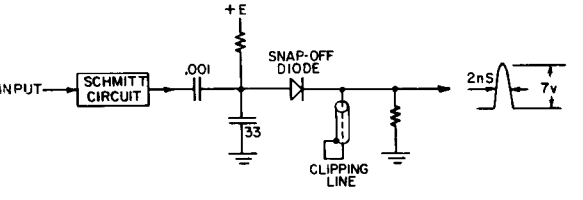


FIGURE 18–2.—Keyed phase detector.

and lower to charge $C_H$ to the amplitude of the signal during the "on" period of $S$. If the output frequency is 100 Mc/sec, a ratio of 100:1 is easily obtained by conventional techniques.

For the unit described, a two-diode bridge with Gallium Arsenide diodes, a holding capacitor of about 20 pf and an input impedance of the dc amplifier of 1 MΩ gave satisfactory results.

The input circuits that generate the sampling pulse determine the noise contribution of the unit inside the lock-loop passband. It is convenient to



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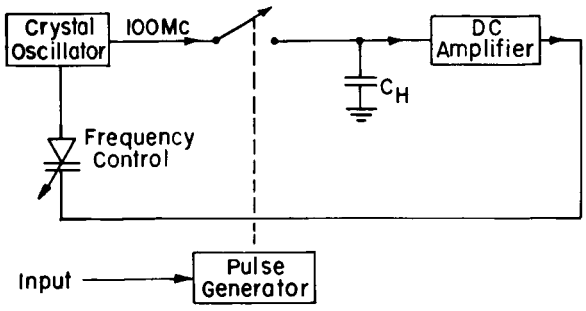


FIGURE 18–3.—Pulse generator.

use an equivalent resistance to describe this noise. This resistance is independent of the multiplication ratio. Several circuit arrangements have been investigated. In all of them, a snap-off (step-recovery) diode generates the pulse (References 2 and 3) for the keyed phase detector. They differ only in the way the input signal, generally a sine wave, drives the snap-off diode. A simple three-stage, overdriven amplifier was used originally but did not provide sufficient squaring at low input frequencies. The next circuit was a Schmitt trigger circuit and amplifier; all data presented in this paper were obtained with this circuit, which accepts a wide range of input frequencies and amplitudes. A tunnel diode circuit can be made more sensitive and can be used at frequencies into the hundreds of megacycles, but allows little range of input amplitude. While the tunnel diode may have somewhat less noise, the experimental use of the multiplier described made it impractical to limit the input amplitude to the 2:1 range of the tunnel-diode circuit. If a multiplier of this type is to be used for output frequencies over a few hundred megacycles, the tunnel diode may be required.

Design parameters of phase-locked oscillators have been treated extensively in the literature and are well understood (References 1 and 4). To understand the requirements of this unit, one need keep in mind only that the phase-locked oscillator will follow the modulating frequency of the controlling signal inside the passband of the lock loop. Outside the passband the noise of the oscillator alone is seen. The phase-lock loop acts as a low-pass filter for noise on the controlling signal and as a high-pass filter for the noise of the locked oscillator. The capture range can be made as wide as the lock range but can be restricted by an additional low-pass filter in the lock loop. If a multiplier is to be used to evaluate the performance of the low-frequency source, the capture range must be made as wide as possible (i.e., the frequency response of the lock loop should not be limited by anything but the lock range of the oscillator which, in turn, should be as wide as possible). Figure 18–4 shows the static characteristic of the 100-Mc crystal oscillator. The usable range is about ±100 ppm.

Figure 18–5 shows the overall response of a multiplier lock loop and the test setup for the measurement. A 5-Mc signal is multiplied to 100 Mc/sec in one channel. The same 5-Mc signal is fed to the other multiplier channel through a phase modulator. The two 100-Mc signals are connected to a phase detector, and the output is recorded as a function of the modulating frequency. The response is flat to about 9 kc/sec (−3 db) and rolls off at 20 db/decade beyond

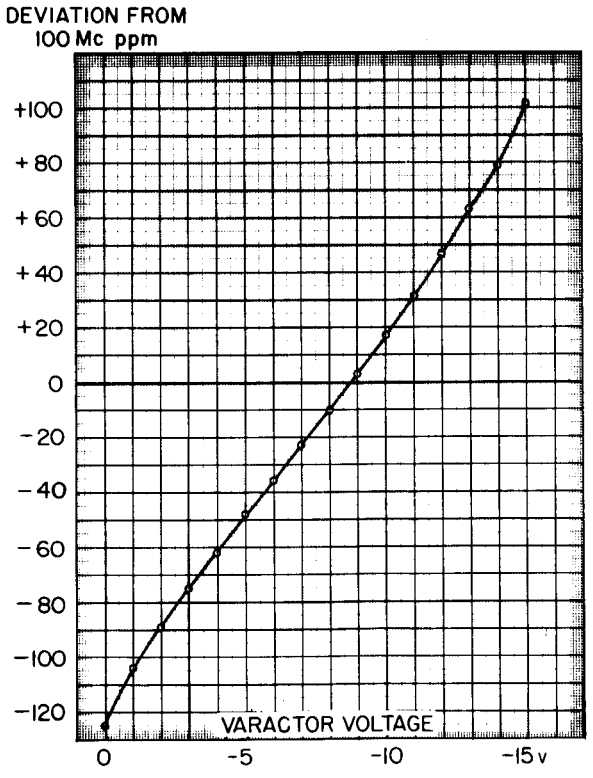


FIGURE 18–4.—Static characteristic voltage-controlled 100-Mc crystal oscillator.

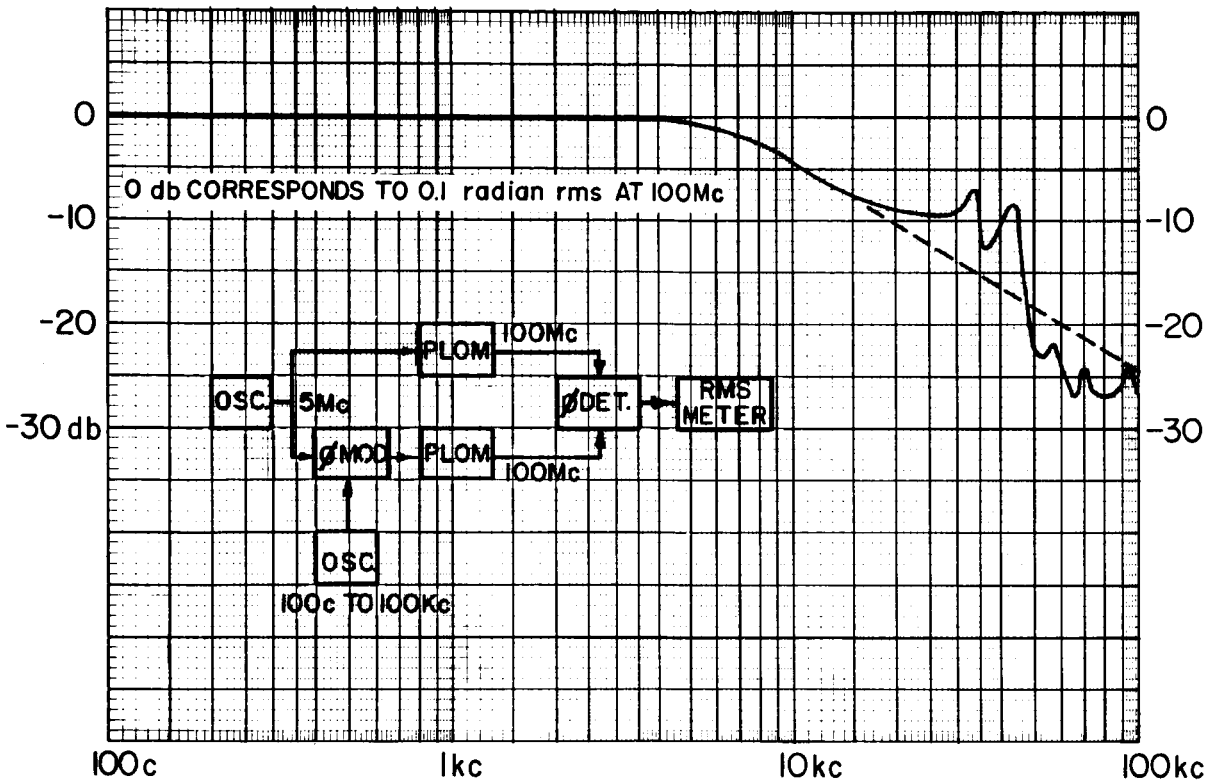


FIGURE 18–5.—Overall response of phase-lock loop of PLOM.

10 kc/sec. The peaks at 34 and 44 kc/sec are caused by spurious modes of the 100-Mc crystal in the locked oscillator. Figure 18–6 shows the spurious responses of the crystal alone. The main mode, at 100 Mc/sec, has a series resistance of 90 ohms; the nearest spurious mode at +34 kc/sec is 800 ohms; and the next, at +44 kc/sec, about 450 ohms.

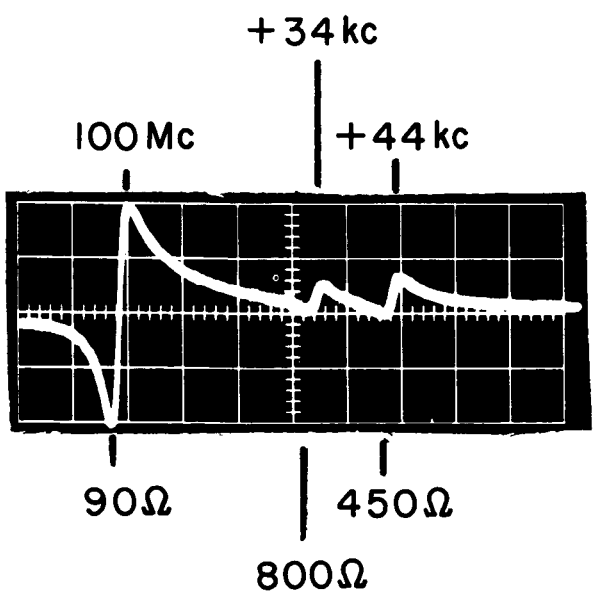


FIGURE 18–6.—Spurious modes of 100-Mc crystal.

## EVALUATION OF PERFORMANCE

To determine the noise of the multiplier, coherent drive was applied to two identical multipliers; and the outputs were compared. Noise common to both inputs does not appear as output if the two multiplier channels have similar characteristics, whereas noise introduced by the multipliers shows up in the output. A wave analyzer can be used to plot the noise spectrum. At the 100-Mc

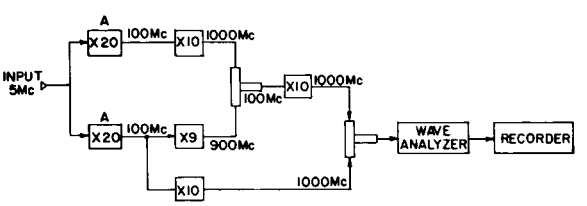


FIGURE 18–7.—Measuring system for noise tests.

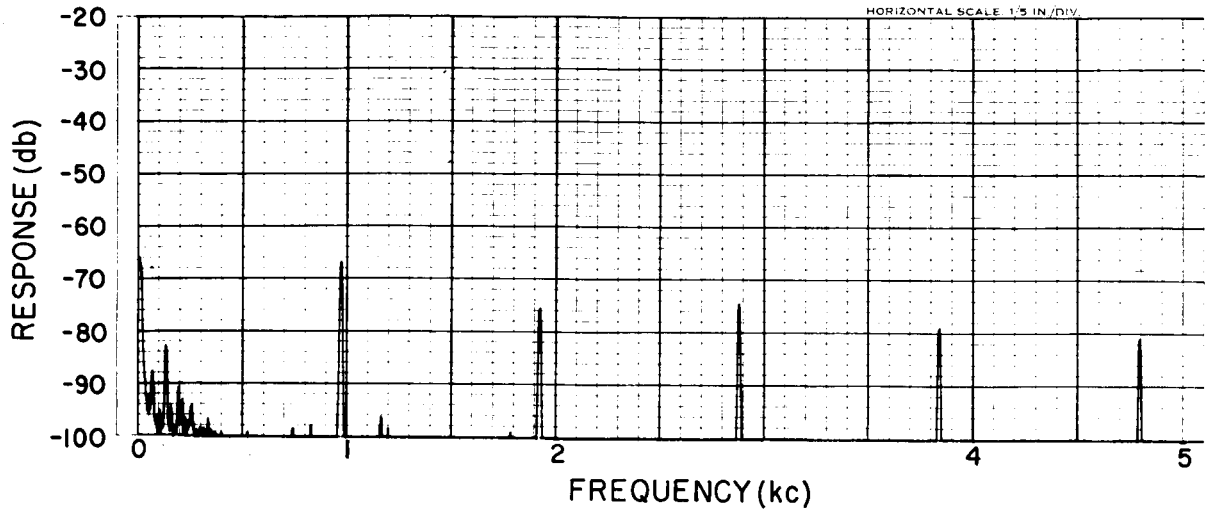


FIGURE 18–8.—X-band spectrum of klystron multiplier only. 100-Mc coherent drive; analyzer bandwidth, 10 c.

output of the phase-locked oscillator multipliers, the noise is too low to be measured, and additional multiplication is required. Figure 18–7 is a block diagram of the setup used for this purpose. This system multiplies phase deviations by 100 so that the spectrum is that which would be obtained at X-band. The multipliers in Figure 18–7 are phase-locked klystron multipliers with 100-kc bandwidth in their lock loops. Unfortunately, these units introduced rather strong sidebands at their power frequency. To separate these sidebands from anything that might be introduced by the phase-locked oscillator multipliers under test, the primary power was obtained from a power oscillator of about 1 kc/sec rather than from 60 cps. The spectrum of Figure 18–8 shows the output from the klystron multipliers with coherent 100-Mc drive to both chains (0 db corresponds to 1 v rms). Note the absence of noise down to the −100 db level except at the low-frequency end. The low-frequency components are caused by a combination of $1/f$ noise in the mixer, direct pickup of 60 and 120 cps through ground loops, and carrier unbalance in the wave analyzer. Relatively strong components are present at the 1-kc power frequency and its harmonics.

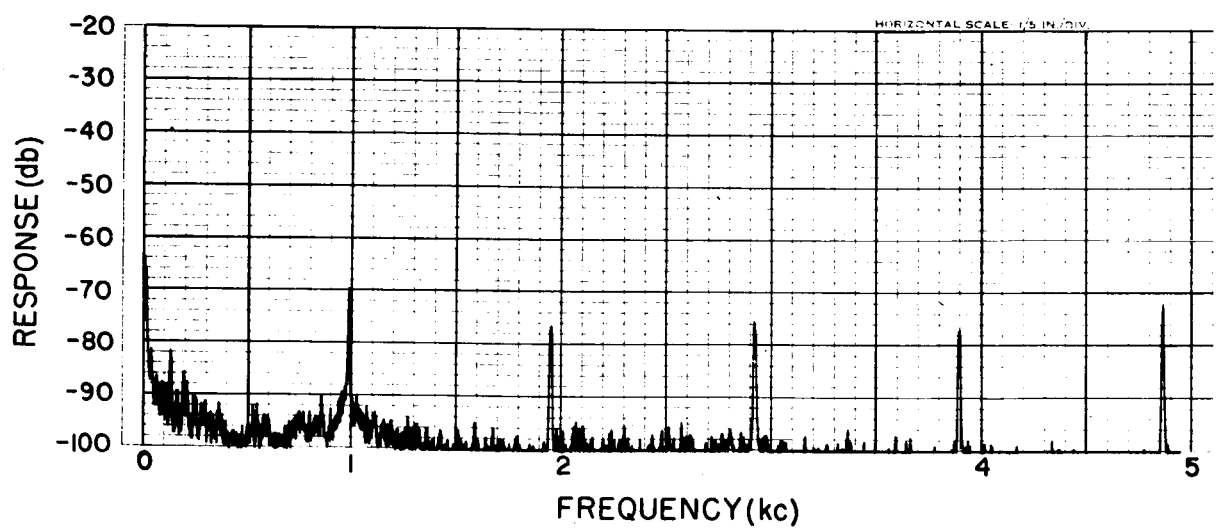


FIGURE 18–9.—X-band spectrum of complete system with 5-Mc coherent drive to PLOMs. Analyzer bandwidth, 10 c.

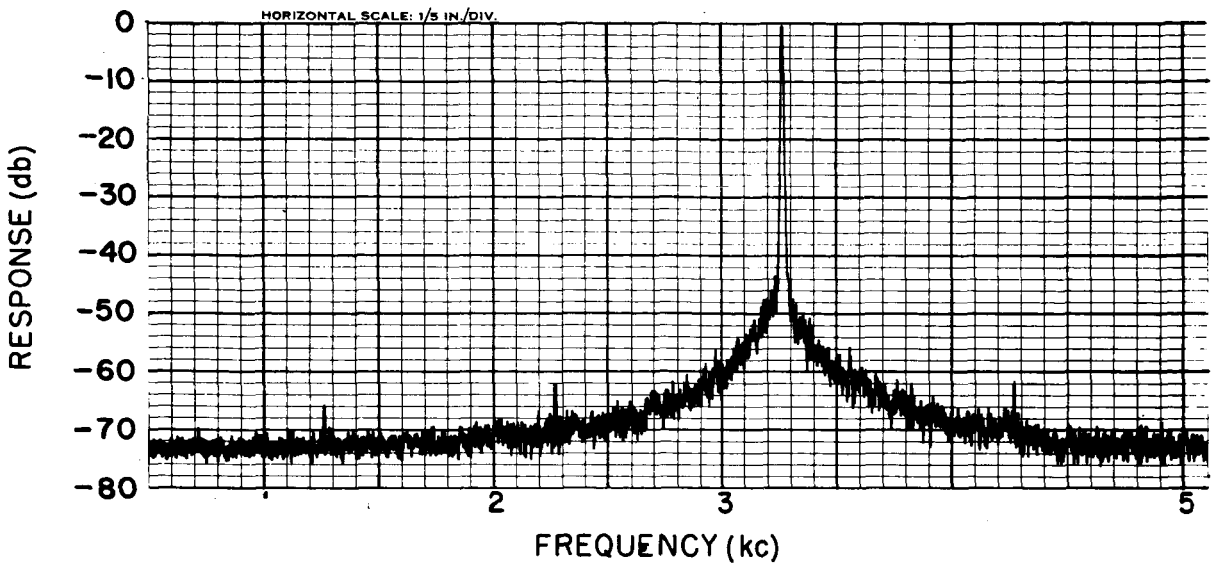


FIGURE 18–10.—X-band spectrum of two 5-Mc oscillators. Analyzer bandwidth, 10 c.

Figure 18–9 shows a spectrum obtained with coherent 5-Mc drive to the two phase-locked oscillator multipliers. The noise level is increased slightly and is between −96 db at a few hundred cps and −100 db above 3 or 4 kc/sec. This is the output from two equally noisy devices and corresponds to −99 to −103 db for one unit. As the spectrum was obtained with 10-cycle bandwidth, another 10 db must be subtracted to get the noise level for a 1-cycle bandwidth, so that the noise at X-band is between −109 and −113 db per cycle bandwidth. This can be reduced to −149 to −153 db referred to the 100-Mc output from the phase-locked oscillator multipliers, or to −175 to −179 db per cycle bandwidth for the 5-Mc input. Expressed in terms of equivalent noise resistance at the multiplier input terminal, the noise is less than that generated by a 200-ohm resistor at 300°K.

A typical application for these multipliers is the measurement of the noise spectrum of two 5-Mc precision sources with crystal drive levels of about 0.7 microwatt. Figure 18–10 shows a typical X-band spectrum.

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